

# EXHIBIT Q

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## PART III of III



## SEAJ Feb. B/B at 0.85

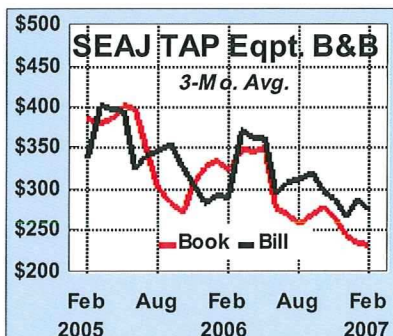
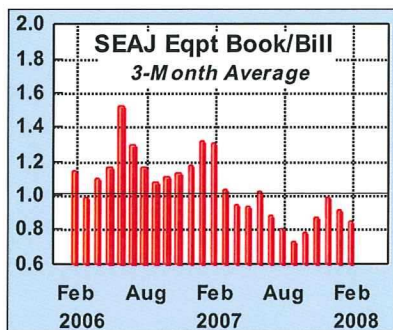
The SEAJ said Japan's chip equipment makers reported ¥112,493 million (US\$1,029.02) in orders in February 2008 (three-month average basis). The bookings figure was down 11.0 percent from the final January 2008 level of ¥126,424 million (US\$1,143.07) and 42.5 percent down from the ¥195,575 million (US\$1,650.93) in orders posted in February 2007.

The three-month average of billings in February 2008 was ¥132,322 million (US\$1,210.40), down 4.3 percent from January 2008 level of ¥138,219 million and 11.6 percent down the February 2007 billings level of ¥149,632 million (US\$1,253.87). The resulting February book-to-bill ratio was 0.85, down from 0.91 in January and below unity for the eighth consecutive month.

In comparison SEMI reported 3-month average bookings by No. American equipment suppliers were \$1,228.9 million for February, up 7.7 percent MoM, but down 12.1 percent YoY. Billings were \$1,315.2 million in February, up 2.8 percent MoM, but down 7.6 percent YoY. SEMI's book-to-bill ratio was 0.93.

### JAPANESE ATE STOCKS

INDEX	Ticker	Close 03/31	Change Month
NIKKEI 225	N225	12,526	-7.9%
Advantest	6857	2,585	-2.3%
JEM	6855	856	-3.2%
MJC	6871	3,190	-8.1%
TEL	8035	6,060	-8.2%
TSK	7729	1,830	-6.3%
Yokogawa	6841	998	-9.4%
Average Change in February			-6.2%



## Japan TAP February Eqpt. B/B at 0.85

Japan's Test, Assembly and Packaging (TAP) equipment makers reported actual bookings for February of ¥25,850 billion (US\$241.0 million), up 8.7 percent MoM but down 28.3 percent YoY. Actual billings were ¥24,814 billion (US\$232.4 million), up 0.6 percent MoM, but down 16.5 percent YoY.

On a three-month average basis, Japan-based TAP equipment makers February bookings were ¥25.379 billion (US\$232.15 million), down 4.3 percent MoM, and down 30.0 percent YoY. Three-month average billings were ¥30,019 billion (US\$274.60 million), up 4.9 percent MoM and down 8.6 percent YoY. The resulting book-to-bill ratio for Japan TAP makers was 0.85 for February 2008.

In comparison, Semi reported that No. America-based Test, assembly and packaging (TAP) equipment bookings were \$220.7 million in February up 6.9 percent MoM up 15.9 percent YoY. Billings were \$201.6 million, up 6.9 percent MoM, but down 1.7 percent YoY. Semi's TAP B/B was 1.09.

## '07 Global Chip Eqpt Revenues Hit \$42.8 B

SEMI and SEAJ reported that worldwide sales of chip totaled \$42.77 billion in 2007, up 5.7 percent YoY, about twice the estimated chip revenues growth. Stanley Myers, president/CEO of SEMI, noted that last year equipment sales to Taiwan surpassed those to Japan and the China new equipment market is rapidly approaching the size of Europe's new equipment market - even as sales in Europe increased by 8 percent.

For the first time, the Taiwan market region spent more semiconductor equipment than any other region, growing 46 percent over 2006 to reach US\$10.65 billion. Japan claimed the number two spot with \$9.31 billion in equipment sales. South Korea ascended to third place reaching \$7.35 billion, passing North America at \$6.55 billion. The Rest of World region, which aggregates Singapore, Malaysia, Philippines, other areas of Southeast Asia and smaller global markets, fell by 18 percent.

The global wafer processing equipment market segment increased 11 percent; the assembly and packaging segment grew 15 percent. But, the total test equipment sales decreased 21 percent YoY. Other front end, which includes mask/reticle equipment, fabrication facility, and wafer manufacturing equipment increased two percent, SEMI said.

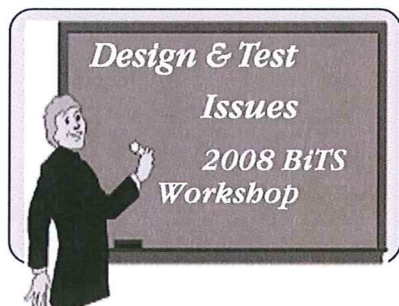
## '06-'07 Chip Eqpt. Market by Region

US \$Million

Region	2006	2007	YoY
China	2,315	2,922	26.2%
Europe	3,595	2,940	-18.2%
Japan	9,209	9,310	1.1%
So. Korea	7,014	7,352	4.8%
N. America	7,324	6,548	-10.6%
Taiwan	7,308	10,648	45.7%
ROW	3,709	3,045	-17.9%
Total	40,474	42,765	5.7%

Source: SEMI-SEAJ





There was plenty for everyone at the 2008 and 9th annual Burn-in & Test Sockets Workshop (BiTS) regardless of their specialty within package test and burn-in. It featured a full technical program of paper presentations, posters, tutorials, prominent speakers and an EXPO featuring products and services from leading suppliers. It also offered an extensive social program to promote networking.

The sold-out EXPO brought the latest products and services from 60 exhibitors to the 350 attendees (30 percent international) and the more than 150 exhibit-only participants.

The technical program's featured speakers delivered important talks on trends in packaging. Dr. Belgacem Haba, Fellow and CTO of Advanced Packaging and Interconnect at Tessera delivered the Invited Talk, while Dr. Karl J. Johnson, VP/Senior Fellow of the Advanced Packaging Systems Integration Laboratory at Freescale Semiconductor was the Keynote Speaker. Filling out the technical program were 26 paper presentations across 8 sessions, and 9 posters in 2 poster sessions.

There were also two tutorials. Ann Swift, Senior Reliability Engineer at IBM Microelectronics opened the Tutorial program with *Basic Chip Reliability Concepts*. This was followed by *"Intellectual Property: What Is It and What Do I Do With It?"* by Ira Blecker, Esq., a Patent Attorney with the Law Offices of Ira D. Blecker.

BiTS was held at the Hilton Phoenix East /Mesa Hotel in Mesa, AZ and included meals, receptions, a casino/karaoke party with a casino, karaoke & hors d'oeuvres, and, of course, the warm Arizona sun.

"An integral part of BiTS is to complement the technical program and EXPO with a social program that encourages networking", said Fred Taber, the BiTS Workshop's General Chair.

Dr. Karl Johnson spoke to the "challenges that are going to be facing the semiconductor industry with respect to packaging and assembly" in his keynote address *Packaging & Assembly in Pursuit of Moore's Law and Beyond*. He note that "over the history of the semiconductor industry the magic was felt to be in the silicon, silicon processing and in the design" but that now "as we continue to move down Moore's Law in the world of digital silicon, the assembly technology and packaging technology are now becoming an integral part of the overall system".

He emphasized that today "you cannot develop your silicon solution without a clear understanding of how your assembly technologies and your packaging are going to influence the overall performance of your system." He concluded by saying that "the market demands of systems Integration with increasing functionality, time to market, flexibility, reuse and 'cost, cost, cost' are necessitating a revolution in packaging and assembly technologies."

Dr. Belgacem Haba then took the audience on a tour of the latest 3D packaging technologies with his invited talk, *Catching the Mobile Wave: Packaging is Going 3D*. Pointing out that silicon consumes a small fraction of the space in a product and that the rest is packaging, he highlighted that "stacking as many die as possible in the Z-direction enables more silicon in less space thus smaller and lighter products with more function."

In closing, Dr. Haba noted that complex testing schemes would need to arise to handle the challenges of 3D packages that are thinner, with tighter I/O pitches (and contacts on the top and bottom), and often are multi-die with more embedded passives.

During the 8 Technical Sessions and 2 poster sessions, authors from across socketing and related industries shared their recent work on a broad range of topics. Among award-winning papers and posters were :

Best Paper; *Optimized Air Cooled Test Socket* -- Grant Wagner, David Gardell; IBM Microelectronics

Best Poster; *Complete Z0= 50 Ohm Coaxial Spring Probe IC Socket* -- Tatsumi Watabe; S.E.R. Corp.

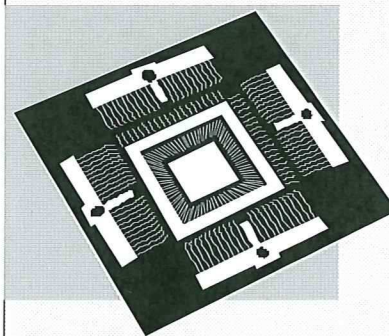
Best Data *New Concept in Spring Probe Design* -- John Winter, Larre Nelson, Amos Friedner; Rika Denshi.

Best Tutorial; *Thermal Design and Analysis* Harlan Faller; Johnstech

Most Inspirational: *Batting Cleanup: Approaches to Maintenance of WLCSP Probe Card Interposers* Jon Diller, Jamie Andes ; Interconnect Devices.

Attendee Choice *"CO2 Composite Spray Technology For Test Socket Cleaning"* David Jackson; Cool Clean Technologies

## ATE/DFT MEETINGS



**June 4 - 6**

*Global STC Conference*  
Hilton Hotel Mission Valley  
San Diego, CA  
<http://www.semitest.org>

**June 8 - 11, 2008**

*SW Test Workshop*  
Paradise Point Resort  
San Diego CA  
<http://www.swtest.org>

**June 8 - 13, 2008**

*Design Automation Conf*  
Anaheim Convention  
Anaheim, CA  
<http://www.dac.com>





## FREDDY'S TEST REPORT

### INDUSTRY



The SIA said WS chip sales (3-month avg.) in February were \$20.44 billion, up 1.5% YoY, but down 4.9% MoM.

Industry Forecasters cut estimates for 2008 chip sales growth.

- **Gartner-Dataquest** cut its IC forecast by half from its December estimate. It now expects the IC market to grow by just 3.4% YoY in 2008.
- **In-Stat** now believes that demand for chips will soften in 2008 growing just 2.4 YoY to \$261.9.
- **IC Insights** stuck with its forecast of 9 percent IC market growth for all of 2008, but said the Q1 results will reveal more about the outlook.

### COMPANIES

**Electrogilas** announced that it has been awarded a patent for its proprietary *Microtouch* probe card impact control algorithm.

**Galaxy Semiconductor Solutions** said **Freescale Semiconductor** has selected its *PAT-MAN* Characterization - a software solution for Part Average Testing (PAT) and related dpm reduction techniques.

**Eagle Test** and **Ismeca Europe Semiconductor SA** announced plans to partner to provide integrated Final Test solutions for Index Parallel Testing of Discrete Devices.

**Wentworth Laboratories**, announced a new vertical probe card solution - *Micromax* - for pre-bump flip chips or aluminum bond pads as an alternative to cantilever type probe cards

**Cadence Design Systems** has acquired **Chip Estimate** (Cupertino, CA), a provider of IC planning and enterprise-level IP reuse management solutions. Terms of the acquisition were not announced.

**Synopsys** will acquire **Synplicity** (Sunnyvale CA), a provider of programmable gate array (FPGA) and IC design and verification solutions, for approximately \$188 million.

### PEOPLE

**Sergio Perez** has joined **SV Probe** as its Sr. VP of Business Development. He has held management positions at **Teradyne**, **Advantest** and most recently at **FormFactor** and was involved in the founding of the **Semi Test Consortium (STC)**.

**Jean Bernard Vernet** has been named CFO for **FormFactor**. He was previously director of risk and assistant treasurer of **Rio Tinto's** aluminum product group. He replaces **Ronald C. Foster**, who joined **Micron Tech.** as CFO/VP of Finance

**Kenneth Levy**, retired CEO /Chairman, and currently Chairman Emeritus of **KLA-Tencor** and **NICE Systems** CEO **Haim Shani** have joined the board of **OptimalTest**

**Hal Lasky** has joined **STATS ChipPAC** as Exec. VP/ Chief Sales Officer, based in the U.S. Prior to joining **STATS ChipPAC**, Lasky spent 24 years at **IBM**.

**Gennady Krasnikov**, president/CEO, **Mikron JSC**, (Zelenograd, Russia), has joined the **Global Semiconductor Alliance's EMEA's** (Europe, Middle East, Africa) Leadership Council

**Nigel Dessau** has joined **AMD** as its chief marketing officer he had previously been with **IBM** and **Sun**,

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